ABSTRACT OF THE DISCLOSURE

A semiconductor device at least has a memory cell array. The memory cell array has active regions extending linearly in parallel with one another at predetermined intervals and each containing alternating source and drain regions, gate electrodes orthogonally crossing the active regions between the source and drain regions and each having a floating gate and a control gate laid one upon another, first conductors extending linearly in parallel with the gate electrodes and connected to corresponding ones of the source regions through source contacts, and second conductors connected to corresponding ones of the drain regions through drain contacts.